AMENDMENTS TO THE DRAWINGS

Please amend FIG. 1 by including the legend "PRIOR ART." A replacement sheet is submitted herewith.

REMARKS

Claims 1, 3, and 5-18 remain in the application with claims 1, 3, 5, 8, 11, 14, 17, and 18 having been amended hereby and claims 2 and 4 having been canceled, without prejudice or disclaimer.

Reconsideration is respectfully requested of the objection to the drawings.

Submitted herewith is a Replacement Sheet for FIG. 1 in which the legend "PRIOR ART" has been added.

Reconsideration is respectfully requested of the objections to claim 17 and 18 as containing informalities.

Claim 17 has been amended hereby to set forth in the preamble that the claim teaches a semiconductor memory device.

Reconsideration is respectfully requested of the rejection of claims 1-4, 14, 17, and 18 under 35 U.S.C. 102(e), as being anticipated by *Porter, et al.*

As explained in the present Specification, an exemplary embodiment of the present invention provides a memory device that can output data as a single data rate pattern or a dual data rate pattern. This accomplished by providing first and second circuit paths operating in conjunction with a merged output generator that receives the output signals from the two data paths. Each data path receives a first data bit and includes logical circuit elements that cooperate with signals provided by a control signal generator, shown in FIG. 4. The control signals are based on a plurality of so-called output clock signals such that a first transmission signal pair is provided and a first single data rate signal is provided for the first path and a second transmission signal pair and a second single data rate signal is provided for the second path circuit. In this way, the first and second path circuits produce respective first and second path output signals that are then merged by the merged output generator.

The claims have been amended hereby to emphasize the above-noted features of the exemplary embodiment described in the Specification.

Porter, et al. describes a system that can transfer data at a single data rate or a double data rate, as in the presently claimed invention. As shown in FIG. 2 of

Porter, et al., an odd path and an even path is provided for the data along with a selection mechanism. In double data rate operation, the second piece of data, as selected by the selection mechanism is different than the first piece of data. The selection mechanism is connected to the two data paths and allows selection of a single or double data rate operation.

Even though *Porter, et al.* shows two data paths for use in a double data rate memory system, it is respectfully submitted that *Porter, et al.* is completely silent concerning the features of the present invention in which the signal paths are controlled based on single data rate signals and first and second transmission signal pairs, as in the presently claimed invention. As shown in FIG. 3 of the present application, the single data rate signal is provided to the transistors 318 and 338 and the pairs of transmission signals are provided to the transmission gates 316 and 336.

It is respectfully submitted that no such structure is shown or suggested in *Porter, et al.*

In regard to claim 17, it is respectfully submitted that *Porter, et al.* is completely silent concerning the provision of a control signal generator that generates the first and second single data rate signals, as well as the first and second transmission signal pairs as set forth in amended claim 17.

Reconsideration is respectfully requested of the rejection of claims 5-13, 15, and 16 under 35 U.S.C. 103(a), as being unpatentable over *Porter, et al.*

These dependent claims all depend from independent claim 1 which, for the reasons set forth hereinabove, is thought to be patentably distinct over the cited reference and, for at least those very same reasons, claims 5-13, 15, and 16 are also submitted to be patentably distinct thereover.

Furthermore, it is respectfully submitted that there is no suggestion in *Porter, et al.*, nor in any reference of record, concerning the specific structure of the control signal generator that is positively set forth in the amended claims.

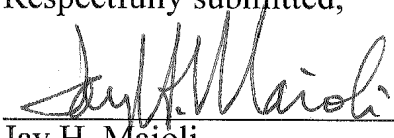
Accordingly, by reason of the amendments made to the claims hereby, as well as the above remarks, it is respectfully submitted that a semiconductor memory device that

can operate either in a single data rate pattern or a dual data rate pattern, as in the presently claimed invention, is neither shown nor suggested in the cited references, alone or in combination.

The references cited as of interest have been reviewed and are not seen to show or suggest the present invention as recited in the amended claims.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,



Jay H. Maioli
Reg. No. 27,213
Attorney for Applicants

Dated: February 22, 2007

Mailing Address:

F. CHAU & ASSOC., LLC
130 Woodbury Road
Woodbury, NY 11797
TEL.: (516) 692-8888
FAX: (516) 692-8889